What Is Claimed Is:

1. A method for speeding up an iterative process that simulates and corrects a layout of a target cell within an integrated circuit so that a simulated layout of a solution for the target cell matches a desired layout for the target cell, the method comprising:

determining if the target cell is similar to a preceding cell for which there exists a previously calculated solution;

if the target cell is similar to the preceding cell, using the previously calculated solution for the preceding cell as an initial input to the iterative process for the target cell; and

performing the iterative process on the target cell to produce the solution for the target cell.

2. The method of claim 1, wherein the target cell is similar to the preceding cell if the layout of the target cell matches the layout of the preceding cell, but the environment surrounding the target cell differs from the environment surrounding the preceding cell.

3. The method of claim 2, wherein if the previously calculated solution for the preceding cell is used as the initial input to the iterative process, the iterative process only operates on features within a border region within the target cell that can be affected by the environment surrounding the target cell, and ignores features within the target cell that are not located within the border region.

4. The method of claim 1, wherein the target cell is similar to the preceding cell if the layout of the target cell matches the layout of the preceding

cell, and the environment surrounding the target cell matches the environment surrounding the preceding cell.

5. The method of claim 1, wherein the simulated layout corresponds to a manufactured result for the layout.

6. The method of claim 1, wherein the target cell is similar to the preceding cell if the layout of the target cell differs from the layout of the preceding cell by less than a pre-specified amount.

7. The method of claim 1, wherein if the previously calculated solution for the preceding cell is used as the initial input for the iterative process, and if the iterative process produces a simulation result that differs significantly from the desired layout, the method further comprises restarting the iterative process using the desired layout instead of the previously calculated solution as the initial input to the iterative process.

8. The method of claim 1, wherein the iterative process involves repeatedly:

simulating a current solution for the target cell to produce a current simulated layout;

if the current simulated layout differs from the desired layout by less than a pre-specified amount, accepting the current solution as a final solution for the target cell; and

otherwise, correcting the current solution to compensate for differences between the current simulated layout and the desired layout.

9. The method of claim 1, wherein prior to considering the target cell, the method further comprises:

receiving a specification for the layout of the integrated circuit; and

dividing the layout into a plurality of cells, whereby each cell can be independently subjected to the iterative process.

10. The method of claim 1, wherein the iterative process performs model-based optical proximity correction (OPC).

11. A computer-readable storage medium storing instructions that when executed by a computer cause the computer to perform a method for speeding up an iterative process that simulates and corrects a layout of a target cell within an integrated circuit so that a simulated layout of a solution for the target cell matches a desired layout for the target cell, the method comprising:

determining if the target cell is similar to a preceding cell for which there exists a previously calculated solution;

if the target cell is similar to the preceding cell, using the previously calculated solution for the preceding cell as an initial input to the iterative process for the target cell; and

performing the iterative process on the target cell to produce the solution for the target cell.

12. The computer-readable storage medium of claim 11, wherein the target cell is similar to the preceding cell if the layout of the target cell matches the layout of the preceding cell, but the environment surrounding the target cell differs from the environment surrounding the preceding cell.

13. The computer-readable storage medium of claim 12, wherein if the previously calculated solution for the preceding cell is used as the initial input to the iterative process, the iterative process only operates on features within a border region within the target cell that can be affected by the environment surrounding the target cell, and ignores features within the target cell that are not located within the border region.

14. The computer-readable storage medium of claim 11, wherein the target cell is similar to the preceding cell if the layout of the target cell matches the layout of the preceding cell, and the environment surrounding the target cell matches the environment surrounding the preceding cell.

15. The computer-readable storage medium of claim 11, wherein the simulated layout corresponds to a manufactured result for the layout.

16. The computer-readable storage medium of claim 11, wherein the target cell is similar to the preceding cell if the layout of the target cell differs from the layout of the preceding cell by less than a pre-specified amount.

17. The computer-readable storage medium of claim 11, wherein if the previously calculated solution for the preceding cell is used as the initial input for the iterative process, and if the iterative process produces a simulation result that differs significantly from the desired layout, the method further comprises restarting the iterative process using the desired layout instead of the previously calculated solution as the initial input to the iterative process.

18. The computer-readable storage medium of claim 11, wherein the iterative process involves repeatedly:

simulating a current solution for the target cell to produce a current simulated layout;

if the current simulated layout differs from the desired layout by less than a pre-specified amount, accepting the current solution as a final solution for the target cell; and

otherwise, correcting the current solution to compensate for differences between the current simulated layout and the desired layout.

19. The computer-readable storage medium of claim 11, wherein prior to considering the target cell, the method further comprises:

receiving a specification for the layout of the integrated circuit; and

dividing the layout into a plurality of cells, whereby each cell can be independently subjected to the iterative process.

20. The computer-readable storage medium of claim 11, wherein the iterative process performs model-based optical proximity correction (OPC).

21. An apparatus for speeding up an iterative process that simulates and corrects a layout of a target cell within an integrated circuit so that a simulated layout of a solution for the target cell matches a desired layout for the target cell, the apparatus comprising:

a comparison mechanism that is configured to determine if the target cell is similar to a preceding cell for which there exists a previously calculated solution;

an iterative processing mechanism that performs the iterative process on the target cell to produce the solution for the target cell;

wherein if the target cell is similar to the preceding cell, the iterative processing mechanism is configured to use the previously calculated solution for the preceding cell as an initial input to the iterative process for the target cell.

22. The apparatus of claim 21, wherein the target cell is similar to the preceding cell if the layout of the target cell matches the layout of the preceding cell but the environment surrounding the target cell differs from the environment surrounding the preceding cell.

23. The apparatus of claim 22, wherein if the previously calculated solution for the preceding cell is used as the initial input to the iterative process, the iterative processing mechanism only operates on features within a border region within the target cell that can be affected by the environment surrounding the target cell, and ignores features within the target cell that are not located within the border region.

24. The apparatus of claim 21, wherein the target cell is similar to the preceding cell if the layout of the target cell matches the layout of the preceding cell, and the environment surrounding the target cell matches the environment surrounding the preceding cell.

25. The apparatus of claim 21, wherein the simulated layout corresponds to a manufactured result for the layout.

26. The apparatus of claim 21, wherein the target cell is similar to the preceding cell if the layout of the target cell differs from the layout of the preceding cell by less than a pre-specified amount.

27. The apparatus of claim 21, wherein if the previously calculated solution for the preceding cell is used as the initial input for the iterative process, and if the iterative processing mechanism produces a simulation result that differs significantly from the desired layout, the iterative processing mechanism is configured to restart the iterative process using the desired layout instead of the previously calculated solution as the initial input to the iterative process.

28. The apparatus of claim 21, wherein the iterative processing mechanism is configured to repeatedly:

simulate a current solution for the target cell to produce a current simulated layout;

if the current simulated layout differs from the desired layout by less than a pre-specified amount, to accept the current solution as a final solution for the target cell; and

otherwise, to correct the current solution to compensate for differences between the current simulated layout and the desired layout.

29. The apparatus of claim 21, further comprising a partitioning mechanism that is configured to:

receive a specification for the layout of the integrated circuit; and to

divide the layout into a plurality of cells, whereby each cell can be independently subjected to the iterative process.

30. The apparatus of claim 21, wherein the iterative processing mechanism performs model-based optical proximity correction (OPC).

31. A mask to be used in an optical lithography process for manufacturing an integrated circuit, wherein the mask is created through a method that simulates and corrects a layout of a target cell within an integrated circuit so that a simulated layout of a solution for the target cell matches a desired layout for the target cell, the method comprising:

determining if the target cell is similar to a preceding cell for which there exists a previously calculated solution;

if the target cell is similar to the preceding cell, using the previously calculated solution for the preceding cell as an initial input to the iterative process for the target cell; and

performing the iterative process on the target cell to produce the solution for the target cell.

32. An integrated circuit created through process that simulates and corrects a layout of a target cell within an integrated circuit so that a simulated layout of a solution for the target cell matches a desired layout for the target cell, the process comprising:

determining if the target cell is similar to a preceding cell for which there exists a previously calculated solution;

if the target cell is similar to the preceding cell, using the previously calculated solution for the preceding cell as an initial input to the iterative process for the target cell; and

performing the iterative process on the target cell to produce the solution for the target cell.

33. A method for jump-starting model-based optical proximity correction, comprising:

receiving a current cell to be subjected to a model-based optical proximity correction process;

analyzing the current cell to identify a previously corrected cell that is similar to the current cell; and

if a similar previously corrected cell is identified, producing an optical proximity correction for the current cell by using an optical proximity correction for the previously corrected cell as an initial optical proximity correction for the current cell.

34. The method of claim 33, wherein the current cell is similar to the previously corrected cell if the layout of the current cell matches the layout of the previously corrected cell, but the environment surrounding the current cell differs from the environment surrounding the previously corrected cell.

35. The method of claim 33, wherein the current cell is similar to the previously corrected cell if the layout of the current cell differs from the layout of the previously corrected cell by less than a pre-specified amount.